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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,512	08/22/2003	Takashi Miyazawa	116908	8756

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EXAMINER	
SHANKAR, VIJAY	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,512	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	VIJAY SHANKAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *1-12 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Applicant's election with traverse of Group I Claims 1-12, 22 in the reply filed on 8-3-2006 is acknowledged. The traversal is on the ground(s) that all Claims have similar subject matters. This is not found persuasive because the both groups have different subject matters claimed.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-12, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Akimoto et al (Us 2003/0067424 A1).

Regarding Claim 1, Akimoto et al teaches an electronic circuit comprising:

first power source line (79 in Figure 10); and

a plurality of unit circuits (70 in Fig.10),

each of the plurality of unit circuits including:

a first transistor (74 in Fig.10) that is coupled to an electronic element and that is coupled to the first power source line (Fig.10; Paragraph 0083-0090);

a second transistor (75 in Fig.10) that controls an electrical connection between a drain of the first transistor and a gate of the first transistor (Fig.10; Paragraph 0083-0090); and

a third transistor (71 in Fig.10) that controls an electrical connection between the first transistor and a current source that outputs a data current that sets a conduction state of the first transistor (Fig.10; Paragraph 0083-0090),

the first power source line (79 in Fig.10) being electrically disconnected from a driving potential during at least a part of a first period in which the third transistor is in an on-state (Fig.10; Paragraph 0083-0090), and

a driving current whose level corresponds to the conduction state of the first transistor set by the data current flowing between the first power source line and the electronic element during at least a part of a second period in which the third transistor is in an off-state (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claim 2, Akimoto et al teaches an electronic comprising a first power source line (79 in Figure 10); and each of the plurality of unit circuit circuits, each of the plurality of unit circuits (70 in Figure 10) including:

a first transistor (74 in Figure 10) that is coupled to an electronic element and that is coupled to the first power source line (Fig.10; Paragraph 0083-0090);

a second transistor (75 in Figure 10) that controls an electrical connection between a drain of the first transistor and a gate of the first transistor (Fig.10; Paragraph 0083-0090); and

a third transistor (71 in Figure 10) that controls an electrical connection between the first transistor and a current source that outputs a data current that sets a conduction state of the first transistor (Fig.10; Paragraph 0083-0090),

the data current flowing through the first transistor during at least a part of a first period in which the third transistor is in an on-state (Fig.10; Paragraph 0083-0090),

a potential of the first power source line being set to a first voltage during at least a part of the first period (Fig.10; Paragraph 0083-0090),

a driving current whose level corresponds to the conduction state of the first transistor set by the data current flowing between the first power source line and the electronic element during at least a part of a second period in which the third transistor is in an off-state (Figures 10,17,20; Paragraph 0083-0090, 0111-0117), and

the potential of the first power source line being set to a second voltage that is different from the first voltage during at least a part of the second period (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claim 3, Akimoto et al teaches an electronic circuit a plurality of unit circuits, each of the plurality of unit circuits including:

a first transistor having a first terminal, a second terminal, and a first control terminal (Fig.10; Paragraph 0083-0090);

a second transistor having a third terminal and a fourth terminal (Fig.10; Paragraph 0083-0090) and

a third transistor having a fifth terminal and a sixth terminal, the fifth terminal being coupled to the first terminal (Fig.10; Paragraph 0083-0090),

the first terminal being coupled to a first power source line; and potential of the first power source line being set to a plurality of potentials or an electrical connection between the first power source line and a driving voltage being controlled. (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claim 4, Akimoto et al teaches an electronic circuit having a plurality of unit circuits, each of the plurality of unit circuits comprising:

a first transistor having a first terminal, a second terminal, and a first control terminal (Fig.10; Paragraph 0083-0090);

a second transistor having a third terminal and a fourth terminal, the third

terminal being coupled to the first control terminal, the second transistor controlling an electrical connection between the second terminal and the third terminal (Fig.10; Paragraph 0083-0090);

a third transistor having a fifth terminal and a sixth terminal, the fifth terminal being coupled to the first terminal (Fig.10; Paragraph 0083-0090); and

a capacitive element having a seventh terminal and an eighth terminal, the seventh terminal being coupled to the first control terminal and the third terminal (Fig.10; Paragraph 0083-0090),

the first terminal being connected to a first power source line together with the first terminals of other unit circuits of the plurality of unit circuits (Fig.10; Paragraph 0083-0090), and

the electronic circuit including a plurality of control circuits, each setting the potential of the first power source line to a plurality of potentials or controlling the supply and the disconnection of a driving voltage to the first power source line. (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claim 5, Akimoto et al teaches an electronic circuit having a plurality of unit circuits, each of the plurality of unit circuits comprising:

a first transistor having a first terminal, a second terminal, and a first control terminal (Fig.10; Paragraph 0083-0090);

a second transistor having a third terminal and a fourth terminal, the third terminal being coupled to the first control terminal, the second transistor controlling

an electrical connection between the second terminal and the third terminal (Fig.10; Paragraph 0083-0090);

a third transistor having a fifth terminal and a sixth terminal, the fifth terminal being coupled to the first terminal (Fig.10; Paragraph 0083-0090); and

a capacitive element having a seventh terminal and an eighth terminal, the seventh terminal being coupled to the first control terminal and the third terminal (Fig.10; Paragraph 0083-0090),

the first terminal being coupled to a first power source line together with the first terminals of other unit circuits of the plurality of unit circuits (Fig.10; Paragraph 0083-0090), and

the eighth terminal being coupled to a second power source line, which is held at a predetermined potential, together with the eighth terminals of other unit circuits of the plurality of unit circuits (Figures 10,17,20; Paragraph 0083-0090, 0111-0117), and

the electronic circuit including a plurality of control circuits, each setting the potential of the first power source line to a plurality of potentials or controlling the supply and the disconnection of a driving voltage to the first power source line. (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claims 6-9 and 22, Akimoto et al teaches an electronic circuit having transistors (Figures 10,17,20; Paragraph 0083-0090, 0111-0117) included in each of the unit circuits including only the first transistor, the second

transistor, and the third transistor (Fig.10); an electronic element being coupled to the second terminal (Figure 10); the electronic element being a current-driven element (Fig.10); each of the control circuits being a fourth transistor having a ninth terminal and a tenth terminal, and the ninth terminal being coupled to the driving voltage, and the tenth terminal being coupled to the first power source line. (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claim 10, Akimoto et al teaches the method of driving an electronic circuit having a plurality of unit circuits, the electronic circuit including first power source lines, each of the plurality of unit circuits comprising:

a first transistor coupled in series to an electronic element and coupled to the first power source line; (Fig.10; Paragraph 0083-0090)

a second transistor that controls an electrical connection between a drain of the first transistor and a gate of the first transistor (Fig.10; Paragraph 0083-0090); and

a third transistor that controls an electrical connection between the first transistor and a current source outputting a data current that sets an electrical connection state of the first transistor (Fig.10; Paragraph 0083-0090),

the method comprising:

a first step of switching the third transistor to an on state to supply the data current to the first transistor to set the electrical connection state of the first transistor (Fig.10; Paragraph 0083-0090); and

a second step of switching the third transistor to an off state and making a current corresponding to the electrical connection state of the first transistor flow between the first power source line and the electronic element (Fig.10; Paragraph 0083-0090),

at least for part of the time period in which in the first step the data current is supplied to the first transistor, the first power source line being electrically disconnected from a driving voltage (Figures 10,17,20; Paragraph 0083-0090, 0111-0117), and

at least for part of the time period in which the second step is performed, the driving voltage being applied to either the drain of the first transistor or the source of the first transistor through the first power source line. (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claim 11, Akimoto et al teaches a method of driving an electronic circuit having a plurality of unit circuits, each of the plurality of unit circuits comprising:

a first transistor having a first terminal, a second terminal, and a first control terminal (Fig.10; Paragraph 0083-0090);

a second transistor having a third terminal and a fourth terminal, the third terminal being coupled to the first control terminal, the fourth terminal being coupled to the second terminal (Fig.10; Paragraph 0083-0090);

a third transistor having a fifth terminal and a sixth terminal, the fifth terminal being coupled to the first terminal; and

a capacitive element having a seventh terminal and an eighth terminal, the seventh terminal being coupled to the first control terminal and the third terminal (Fig.10; Paragraph 0083-0090),

the first terminal being coupled to a first power source line together with the first terminals of a series of unit circuits of the plurality of unit circuits,

the method comprising:

a step of electrically disconnecting the first terminals of the series of unit circuits from a driving voltage by electrically coupling the first power source line from the driving voltage, causing a quantity of charge corresponding to the current level of a current flowing through the first transistor to be held in the capacitive element by switching the third transistor of each of the series of unit circuits to an on state, and applying a voltage corresponding to the quantity of charge to the first control terminal to set an electrical connection state between the first terminal and the second terminal (Figures 10,17,20; Paragraph 0083-0090, 0111-0117); and

a step of switching the third transistor to an off state and electrically connecting the first terminal of each of the series of unit circuits to the driving voltage. (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

Regarding Claim 12, Akimoto et al teaches amethod of driving an electronic circuit having a plurality of unit circuits, each of the plurality of unit circuits comprising:

a first transistor having a first terminal, a second terminal, and a first control terminal (Fig.10; Paragraph 0083-0090);

a second transistor having a third terminal and a fourth terminal, the third terminal being coupled to the first control terminal, the fourth terminal being coupled to the second terminal (Fig.10; Paragraph 0083-0090);

a third transistor having a fifth terminal and a sixth terminal, the fifth terminal being coupled to the first terminal (Fig.10; Paragraph 0083-0090); and

a capacitive element having a seventh terminal and an eighth terminal, the seventh terminal being coupled to the first control terminal and the third terminal (Fig.10; Paragraph 0083-0090),

the first terminal being coupled to a first power source line together with the first terminals of a series of unit circuits of the plurality of unit circuits (Fig.10; Paragraph 0083-0090), and

the eighth terminal being coupled to a second power source line together with the eighth terminals of the series of unit circuits of the plurality of unit circuits (Fig.10; Paragraph 0083-0090),

the method comprising:

a step of electrically disconnecting the first terminals of the series of unit circuits from a driving voltage by electrically disconnecting the first power source line from the driving voltage, causing a quantity of charge corresponding to the current level of a current flowing through the first transistor to be held in the capacitive element by switching the third transistor of each of the series of unit circuits to an on state, and applying a voltage corresponding to the quantity of charge to the first

control terminal to set an electrical connection state between the first terminal and the second terminal (Figures 10,17,20; Paragraph 0083-0090, 0111-0117); and

a step of switching the third transistor to an off state and electrically connecting the first terminal of each of the series of unit circuits to the driving voltage. (Figures 10,17,20; Paragraph 0083-0090, 0111-0117).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIJAY SHANKAR
Primary Examiner
Art Unit 2629

VS